WHAT IS CLAIMED IS:

1. A method of forming a via contact structure, the method comprising the steps of:

forming a lower interconnection line on a semiconductor substrate;

forming an inter-metal dielectric layer and a hard mask layer on an entire surface of the semiconductor substrate having the lower interconnection line;

patterning the hard mask layer and the inter-metal dielectric layer to form a via hole exposing the lower interconnection line;

forming a sacrificial layer filling the via hole on the hard mask layer;

patterning the sacrificial layer and the hard mask layer to form a first sacrificial layer pattern having an opening that crosses over the via hole and a second sacrificial layer pattern that remains in the via hole, and to simultaneously form a hard mask pattern underneath the first sacrificial layer pattern;

partially etching the inter-metal dielectric layer using the hard mask pattern as an etching mask to form a trench crossing over the via hole; and

removing the second sacrificial layer pattern to expose the lower interconnection line.

2. The method according to claim 1 further comprising the step of forming a via etch stop layer on the semiconductor substrate having the lower interconnection line prior to formation of the inter-metal dielectric layer, wherein the via etch stop layer is etched after removal of the second sacrificial layer pattern to form a final via hole that exposes the lower interconnection line.

3. The method according to claim 2, wherein the via etch stop layer is formed of an insulating nitride layer or an insulating carbide layer that has an etching selectivity with respect to the inter-metal dielectric layer.

4. The method according to claim 3, wherein the insulating nitride layer is a silicon nitride layer (SiN), a silicon carbonitride layer (SiCN) or a boron nitride layer (BN), and the insulating carbide layer is a silicon carbide layer (SiC).

5. The method according to claim 1, wherein the inter-metal dielectric layer is formed of a single layer of insulating material, the trench being formed to a depth less than the total thickness of the inter-metal dielectric layer.

6. The method according to claim 1, wherein the inter-metal dielectric layer is formed by sequentially stacking a lower inter-metal dielectric layer, a trench etch stop layer and an upper inter-metal dielectric layer, the trench being formed by etching the upper inter-metal dielectric layer until the trench etch stop layer is exposed.

7. The method according to claim 6, wherein the trench etch stop layer is formed of an insulating nitride layer or an insulating carbide layer that has an etching selectivity with respect to the upper inter-metal dielectric layer.

8. The method according to claim 7, wherein the insulating nitride layer is a silicon nitride layer, a silicon carbonitride layer (SiCN) or a boron nitride layer (BN), and the insulating carbide layer is a silicon carbide layer (SiC).

9. The method according to claim 1, wherein the hard mask layer is formed of an insulating nitride layer, an insulating carbide layer, a metal nitride layer, a metal oxide layer or a silicon layer that has an etching selectivity with respect to the inter-metal dielectric layer and the sacrificial layer.

10. The method according to claim 9, wherein the insulating nitride layer is a silicon nitride layer (SiN), a silicon carbonitride layer (SiCN) or a boron nitride layer (BN), the insulating carbide layer is a silicon carbide layer (SiC), the metal nitride layer is a tantalum nitride layer or a titanium nitride layer, the metal oxide layer is an aluminum oxide layer (Al_2O_3), a tantalum oxide layer or a titanium oxide layer, and the silicon layer is a polycrystalline silicon layer or an amorphous silicon layer.

11. The method according to claim 1, wherein the sacrificial layer is formed of an inorganic material layer.

12. The method according to claim 11, wherein the inorganic material layer is a hydro-silses-quioxane (HSQ) layer formed by using a spin coating technique.

13. The method according to claim 1 further comprising the step of forming an anti-reflective layer on the sacrificial layer before patterning the sacrificial layer and the hard mask layer, wherein the anti-reflective layer is concurrently patterned with the sacrificial layer and the hard mask layer.

14. The method according to claim 1, wherein the step of patterning the sacrificial layer and the hard mask layer comprising the sub-steps of:

forming a photoresist pattern on the sacrificial layer, the photoreisst pattern having an opening that crosses over the via hole;

etching the sacrificial layer using the photoresist pattern as an etching mask to form the first sacrificial layer pattern having an opening that crosses over the via hole and the second sacrificial layer pattern that remains in the via hole;

removing the photoresist pattern; and

etching the hard mask layer using the first sacrificial layer pattern as the etching mask to form the hard mask pattern underneath the first sacrificial layer pattern.

15. The method according to claim 1, wherein the step of patterning the sacrificial layer and the hard mask layer comprising the sub-steps of:

forming a photoresist pattern on the sacrificial layer, the photoreisst pattern having an opening that crosses over the via hole;

successively etching the sacrificial layer and the hard mask layer using the photoresist pattern as an etching mask to form the first sacrificial layer

pattern having an opening that crosses over the via hole the second sacrificial layer pattern that remains in the via hole, and to simultaneously form the hard mask pattern underneath the first sacrificial layer pattern; and

removing the photoresist pattern.

16. The method according to claim 1 further comprising the steps of:

forming an upper metal layer filling the via hole and the trench on the hard mask pattern after removal of the second sacrificial layer pattern; and

planarizing the upper metal layer to form an upper metal interconnection line that fills the via hole and the trench.

17. The method according to claim 16, wherein the upper metal layer is formed by sequentially stacking a diffusion barrier layer and a metal layer.

18. A method of forming a via contact structure, the method comprising the steps of:

forming a lower interconnection line on a semiconductor substrate;

sequentially forming a via etch stop layer, a lower inter-metal dielectric layer, a trench etch stop layer, an upper inter-metal dielectric layer and a hard mask layer on an entire surface of the semiconductor substrate having the lower interconnection line;

successively patterning the hard mask layer, the upper inter-metal dielectric layer, the trench etch stop layer and the lower inter-metal dielectric

layer to form a preliminary via hole that exposes the via etch stop layer on the lower interconnection line;

forming a sacrificial layer filling the preliminary via hole on the hard mask layer;

patterning the sacrificial layer and the hard mask layer to form a first sacrificial layer pattern having an opening that crosses over the preliminary via hole and a second sacrificial layer pattern that remains in the prelimianry via hole, and to simultaneously form a hard mask pattern underneath the first sacrificial layer pattern;

etching the upper inter-metal dielectric layer using the hard mask pattern and the trench etch stop layer as an etching mask and an etch stop layer respectivley, thereby forming a trench in the upper inter-metal dielectric layer;

selectively removing the second sacrificial layer pattern to expose the via etch stop layer; and

etching the exposed via etch stop layer to form a final via hole that exposes the lower interconnection line.

19. The method according to claim 18, wherein the via etch stop layer is formed of an insulating nitride layer or an insulating carbide layer that has an etching selectivity with respect to the lower inter-metal dielectric layer.

20. The method according to claim 19, wherein the insulating nitride layer is a silicon nitride layer (SiN), a silicon carbonitride layer (SiCN) or a boron nitride layer (BN), and the insulating carbide layer is a silicon carbide layer (SiC).

21. The method according to claim 20, wherein the trench etch stop layer is formed of an insulating nitride layer or an insulating carbide layer that has an etching selectivity with respect to the upper inter-metal dielectric layer.

22. The method according to claim 21, wherein the insulating nitride layer is a silicon nitride layer, a silicon carbonitride layer (SiCN) or a boron nitride layer (BN), and the insulating carbide layer is a silicon carbide layer (SiC).

23. The method according to claim 18, wherein the hard mask layer is formed of an insulating nitride layer, an insulating carbide layer, a metal nitride layer, a metal oxide layer or a silicon layer that has an etching selectivity with respect to the upper inter-metal dielectric layer and the sacrificial layer.

24. The method according to claim 23, wherein the insulating nitride layer is a silicon nitride layer (SiN), a silicon carbonitride layer (SiCN), or a boron nitride layer (BN), the insulating carbide layer is a silicon carbide layer (SiC), the metal nitride layer is a tantalum nitride layer or a titanium nitride layer, the metal oxide layer is an aluminum oxide (Al_2O_3) layer, a tantalum oxide layer or a

titanium oxide layer, and the silicon layer is a polycrystalline silicon layer or an amorphous silicon layer.

25. The method according to claim 18 further comprising the step of forming an anti-reflective layer on the sacrificial layer before patterning the sacrificial layer and the hard mask layer, wherein the anti-reflective layer is concurrently patterned with the sacrificial layer and the hard mask layer.

26. The method according to claim 18, wherein the step of patterning the sacrificial layer and the hard mask layer comprising the sub-steps of:

forming a photoresist pattern on the sacrificial layer, the photoreisst pattern having an opening that crosses over the preliminary via hole;

etching the sacrificial layer using the photoresist pattern as an etching mask to form the first sacrificial layer pattern having an opening that crosses over the preliminary via hole and the second sacrificial layer pattern that remains in the preliminary via hole;

removing the photoresist pattern; and

etching the hard mask layer using the first sacrificial layer pattern as the etching mask to form the hard mask pattern underneath the first sacrificial layer pattern.

27. The method according to claim 18, wherein the step of patterning the sacrificial layer and the hard mask layer comprising the sub-steps of:

forming a photoresist pattern on the sacrificial layer, the photoreisst pattern having an opening that crosses over the preliminary via hole;

successively etching the sacrificial layer and the hard mask layer using the photoresist pattern as an etching mask to form the first sacrificial layer pattern having an opening that crosses over the preliminary via hole and the second sacrificial layer pattern that remains in the preliminary via hole, and to simultaneously form the hard mask pattern underneath the first sacrificial layer pattern; and

removing the photoresist pattern.

28. The method according to claim 18 further comprising the steps of:

forming an upper metal layer filling the final via hole and the trench on the hard mask pattern after formation of the final via hole; and

planarizing the upper metal layer to form an upper metal interconnection line that fills the final via hole and the trench.

29. The method according to claim 28, wherein the upper metal layer is formed by sequentially stacking a diffusion barrier layer and a metal layer.

30. The method according to claim 16, wherein the hard mask pattern is formed of a conductive layer or a semiconductor layer, the hard mask pattern is removed during or after the planarization process.

31. The method according to claim 28, wherein the hard mask pattern is formed of a conductive layer or a semiconductor layer, the hard mask pattern is removed during or after the planarization process.